



Double Impact Discrete Semiconductor Tester

Devices

- Transistors
- Diodes
- FETs
- JFETs
- Zeners
- IGBTs
- Darlingtons
- MCTs
- SCRs
- Triacs
- Optos
- Small Signal Devices
- Power Semi Components
- Multi Device Packages
- Arrays and Hybrids



Features

- 600 to 2000 Volts
- 20 to 500 Amps
- 5 Station Capability
- Handler Interfaces
- Prober Interfaces
- PC Applications Software
- 0-99 Sort Display
- Flexible Design
- Export Data to Excel
- Statistical Reports
- Hi Rel Reports
- Columnar Reports
- Extensive Test Library
- Easy to Use Software
- Safety Features

The Double Impact tester can test both small signal and power semiconductor devices with repeatable and accurate results. A variety of test stations can accommodate almost any application including incoming inspection, final test, wafer probe, quality control, Hi Reliability and component characterization. The tester is controlled by a Pentium® PC and operates under Windows 98©.

Up to four additional test stations can be added to the mainframe for increased voltage, current or to handle arrays and hybrids.

Test Stations



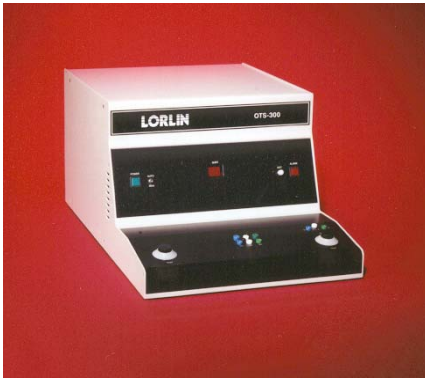
OTS-100 Test Station

- 600 Volt, 20 Amp Standard Test Capability
- 30 Amps with Optional IC Board
- 100 Amps with Optional HCM100 Supply
- Optional Handler or Prober Interface, 25 Bin Capability
- 0-99 Sort Display



HVS-102 Test Station

- 2000 Volt, 20 Amps Standard Test Capability
- Built In 2000 Volt Supply
- 30 Amps with Optional IC Board
- 50 Amps with Optional HCM100 Supply
- Optional Handler or Prober Interface, 25 Bin Capability
- 0-99 Sort Display



OTS300, 340 and HCS-500

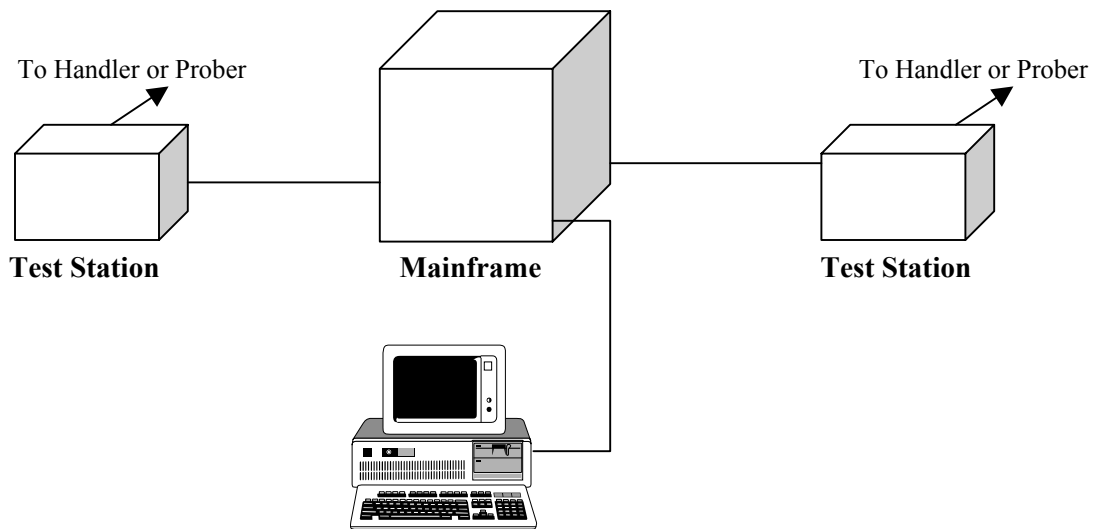
- 200 Amp, 600 Volt Test Station (OTS-300)
- 400 Amps with OTS-340
- 500 Amps with HCS-500
- Built In Power Supply
- Optional Handler or Prober Interface, 25 Bin Capability
- 0-99 Sort Display



SS100 and SS150

- Tests Multi-Device Packages, Arrays, Optos as well as standard components.
- Each SS Station can test up to 10 Devices in a package, both 2 and 3 leads.
- One 3 Pin Board is Standard, Up to 9 additional boards can be added, 30 pins max.
- The SS100 has two versions, 600 or 2000 Volts, both with 20 Amps
- The SS150 offers 600 Volts, 2 Amps and a picoammeter for testing low leakage fets and Jfets. 0 to 200 pA Range, 100 fA resolution.
- Optional Handler or Prober Interface, 25 Bin Capability
- Optional Capacitance Measurement Capability

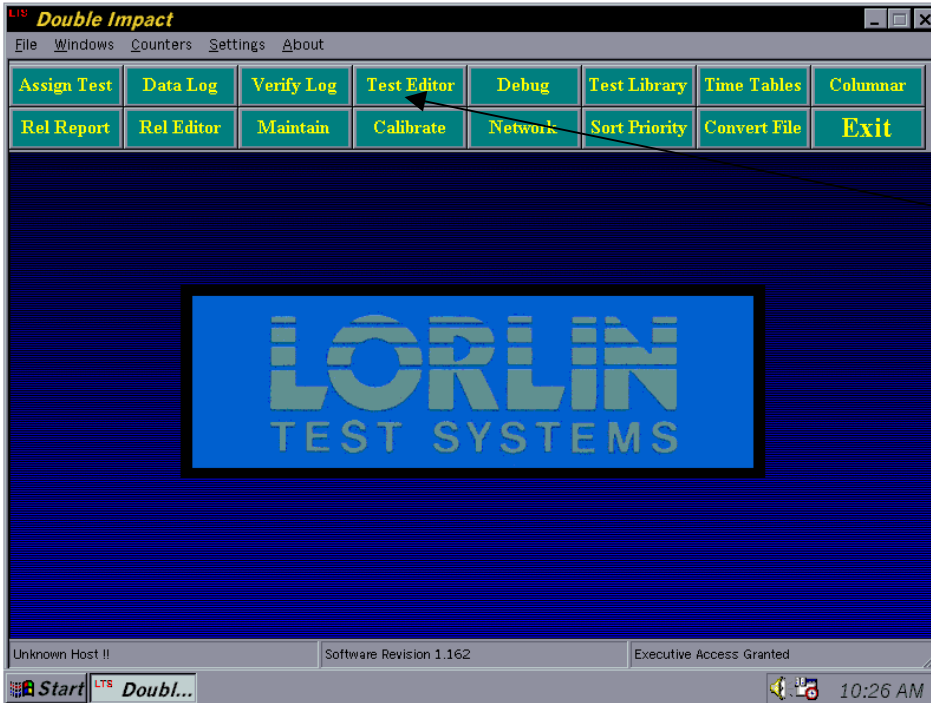
System Configurations



Shown above is a two-station configuration. The system mainframe can be interfaced with up to five test stations total. Manual testing can be performed at both test stations or they can be equipped with the optional handler/prober interface package so automatic testing with handlers and probers can be accomplished at any station. One PC can control all stations or additional PCs can be added for control of each test station as well as viewing datalog information.

The standard test stations offer a 5 pA resolution on leakage measurements without the need for special low current options. Breakdown voltages are performed with a 50 mV resolution. An extensive library of test parameters is offered for testing discrete components. Each station can be set up to run test by branch or test by sort methods of testing concurrently. Test by branch is the most common while test by sort is generally used in manufacturing applications where parts need to be classified.

Software

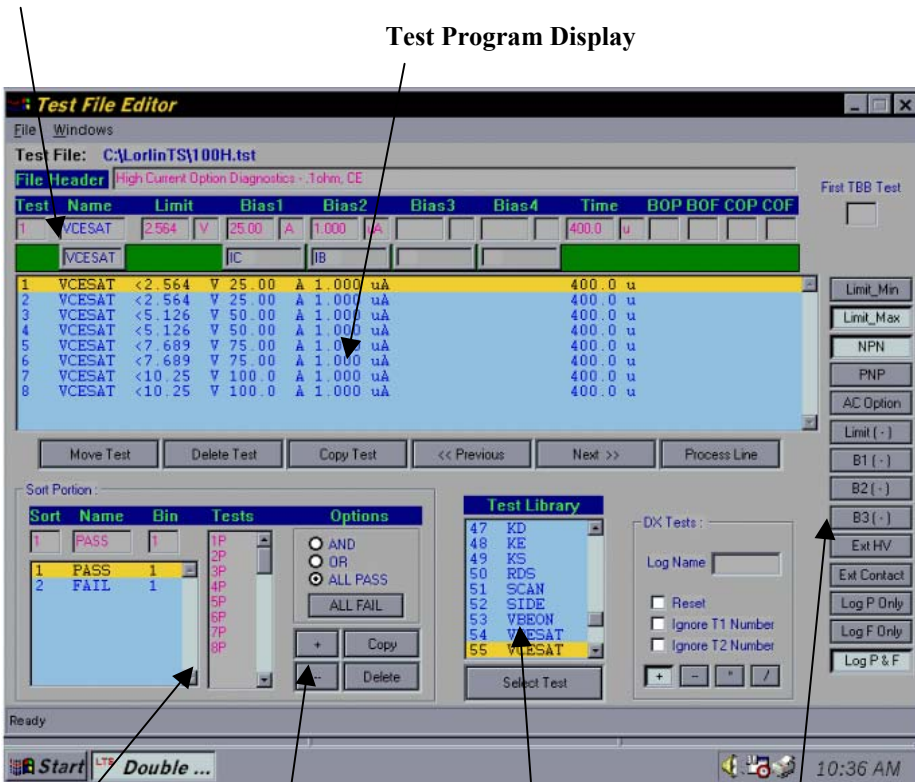


Main Menu

- Easy to Use Windows Menus
- Runs under Windows 98©
- Opening Main Menu Powers Up Tester

Easy Point and Click Selections

Test Line to Enter Data



Test Program Creation

- Create a Test Program Name
- Select Test from the Test Library
- Enter Limit and Bias Values
- Default Test Times Generated
- Adjustable Test Times on the Screen
- Select Process Line to Complete
- Datalogging Modes for Each Test
- Copy Tests or Move Tests Easily
- Scroll Through Tests using Previous and Next
- Branch to next test on Pass, BOP, on Fail, BOF.
- Cover on Pass, COF, or on Fail, COF.

Sort Plan

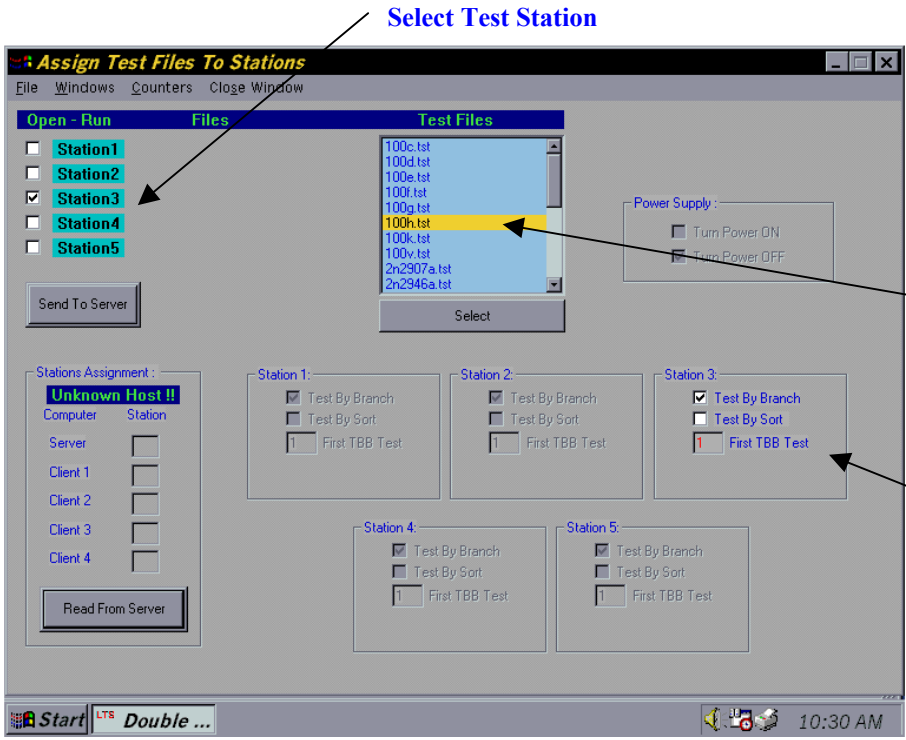
- Easy Sort/Bin Set Up
- Sort by Pass or Fail
- Sort by Individual Parameters
- AND & OR Sort Functions

Sort Plan Set Up

AND OR Functions

Test Library

Master Controls for Each Test



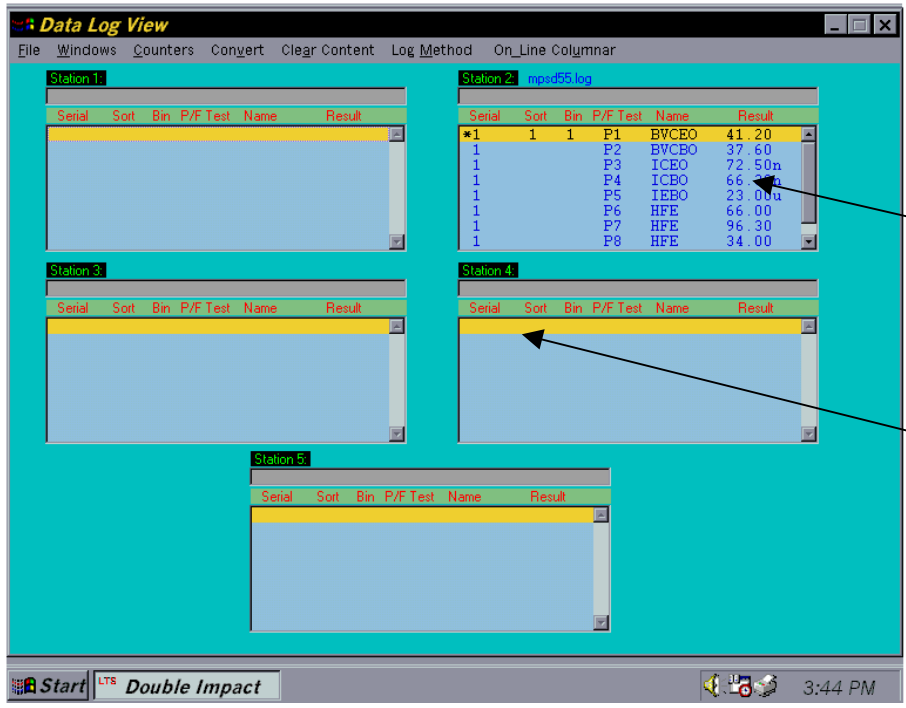
Select Test Station

Set Up Test Stations

- Click on Station
- Click on Test Program
- Station is now Set for Testing

Select Test Program for the Station here.

Set Method of Test TBB or TBS



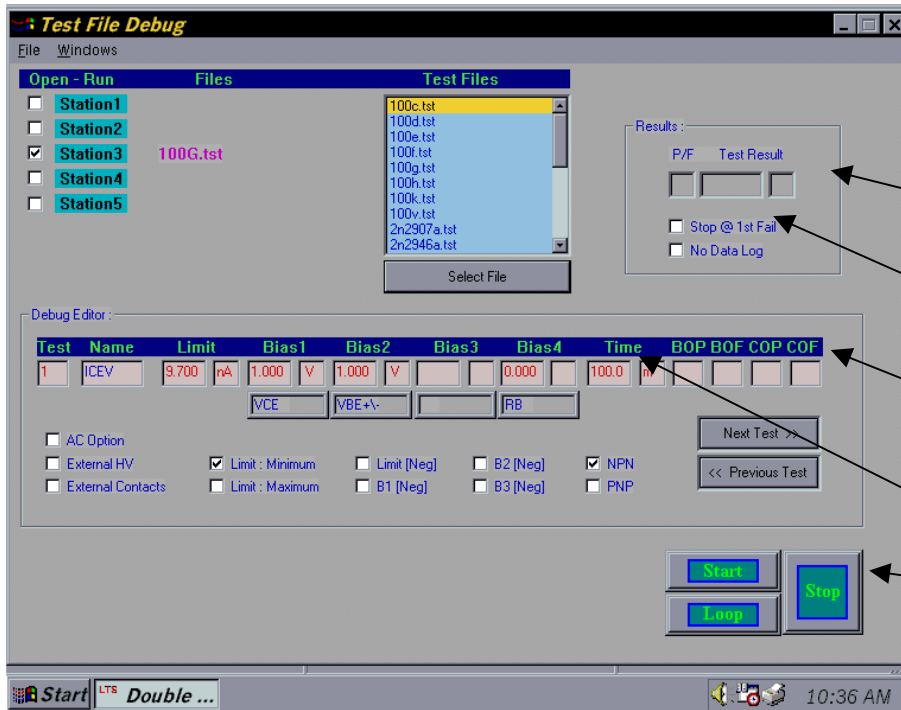
Datalogging

- Create a Datalog File Name
- Data displayed while testing

Test Results

Serial Number, Sort#, Bin# and Pass/Fail Displayed

Test File Debug



- Powerful New Tool
- Helps Fine Tune or “Tweak” Test Routine
- Study Cause and Effect Relationships
- Single Step Through the Test Routine

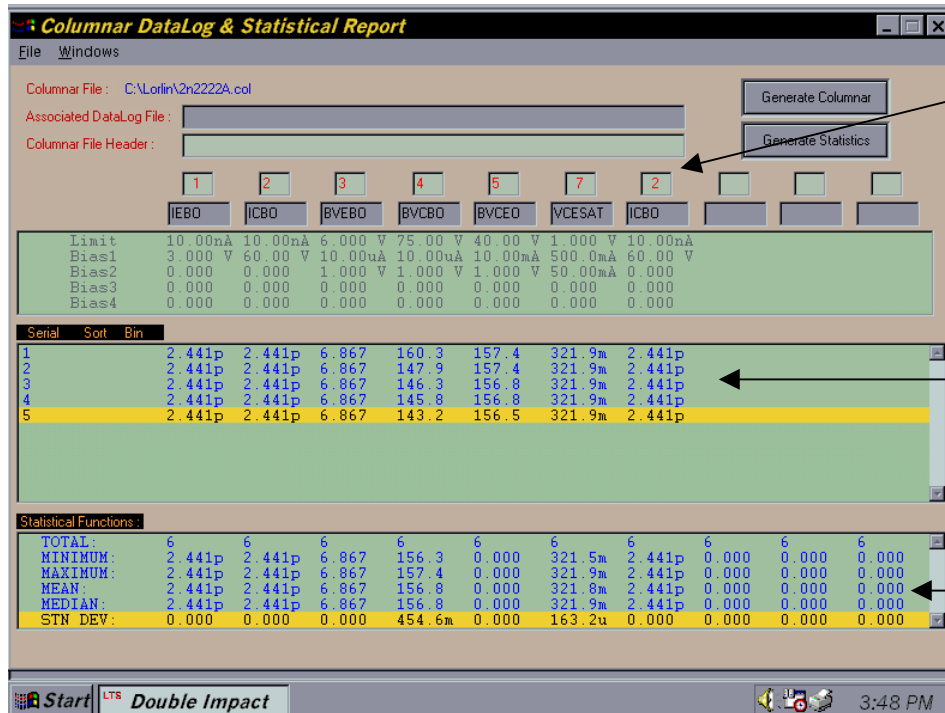
Test Results Displayed Here

Loop on a test until a failure occurs

Scroll Through Test Line and Change Parameters for Each Test

Adjust Test Time and View Results

Initiate Test or Loop on Test

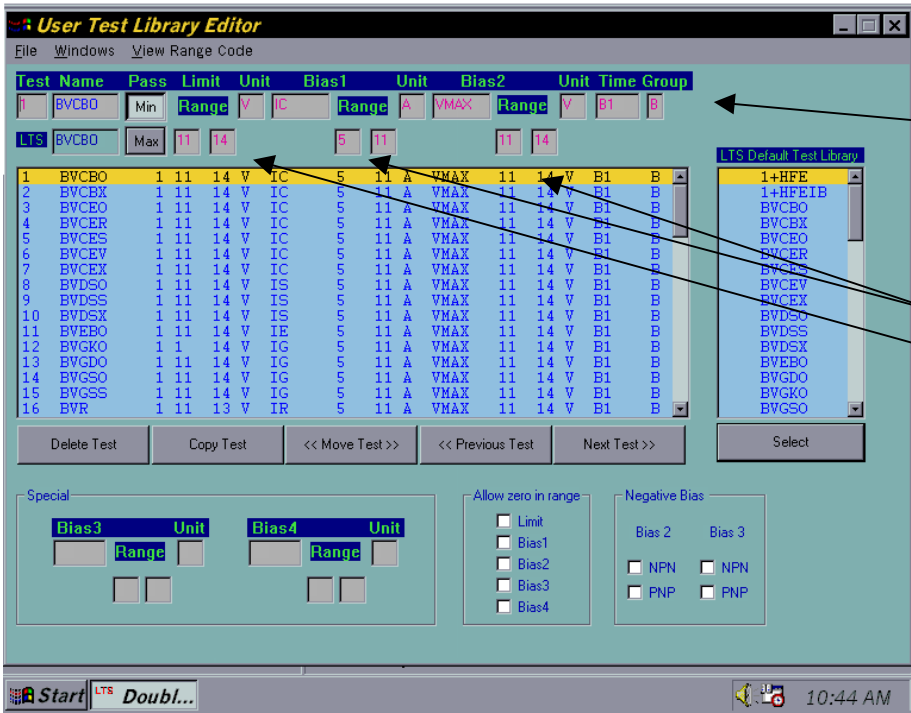


Columnar and Stats

Enter Test Number and Test Name and Data is Displayed

Test Results Are Displayed

Statistical Results Displayed



User Test Library Editor

Rename Tests, Redefine Parameters

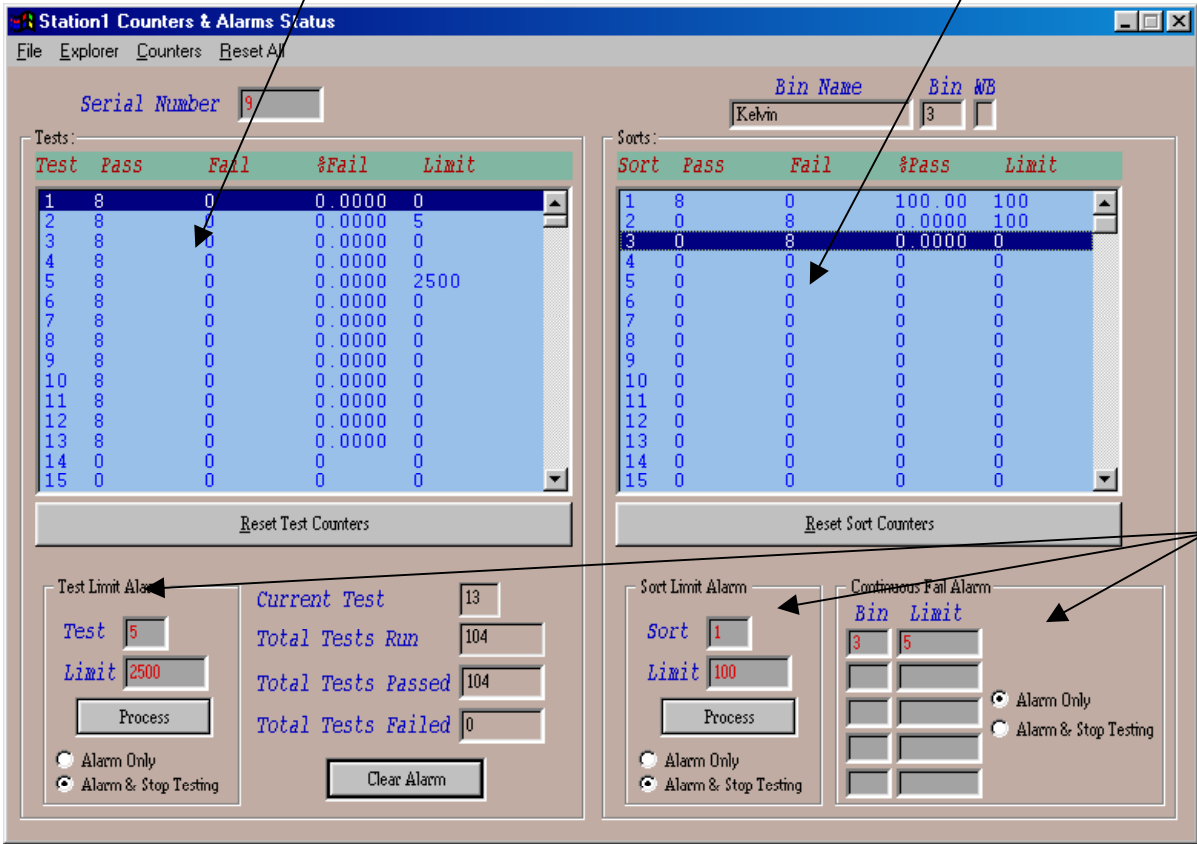
Bias Definitions

Range Definitions

Counters and Alarms

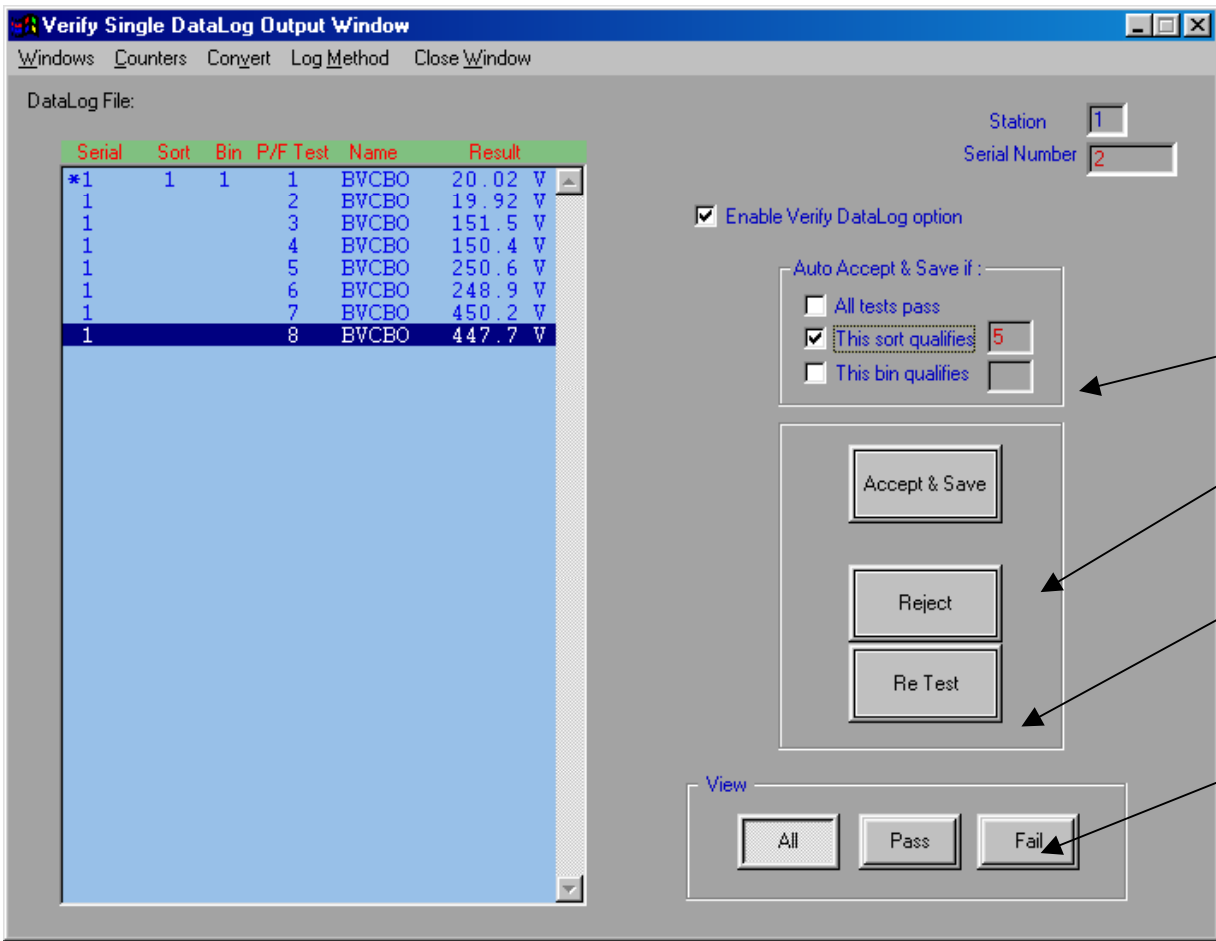
Test Field Displays each test with #Passes, #Fails, and %

Sort Field Displays Sort#, Pass, Fail, %



Set Alarms Features

Alarms can be set as Alarm, or Alarm and Stop Testing



Verify Datalog

Allows complete control of contents of Datalog File and Serial Number of the Parts.

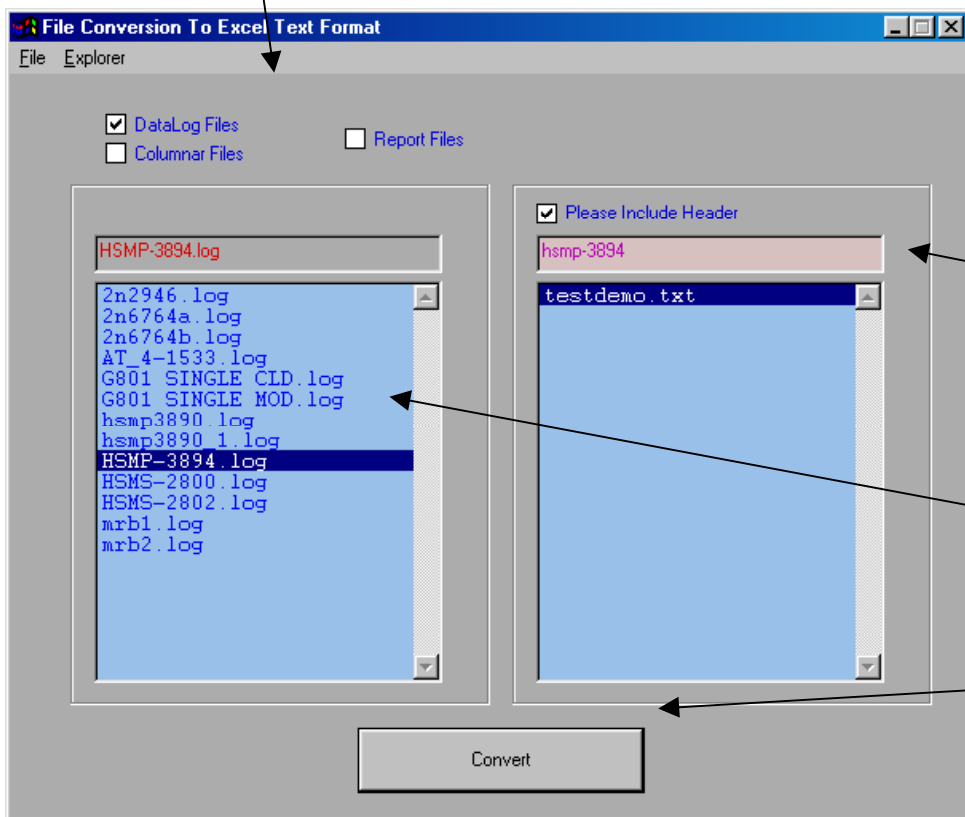
Conditional Auto Save Feature

Accept & Save Data to File

Reject Data and Part from the Lot

Retest and Keep Serial Number

Select Type of Files to Convert



Excel Conversion of Data

Converts Datalog, Columnar, Hi Rel and Report Files.

Converted text files

Datalog Files shown for conversion

Depress Convert Button and Files are Converted Instantly.

Default Test Time Groups A-D
User Defined Time

Table Groups E-H

Test Time Tables

Allows users to easily amend the test time entries.

T1 Status Delay

T2 Power On

T3 Post Delay

Range Define Test Name for Each Group

Datalog Editor Window

Allows users to examine and make changes to existing datalog files that are stored on disk.

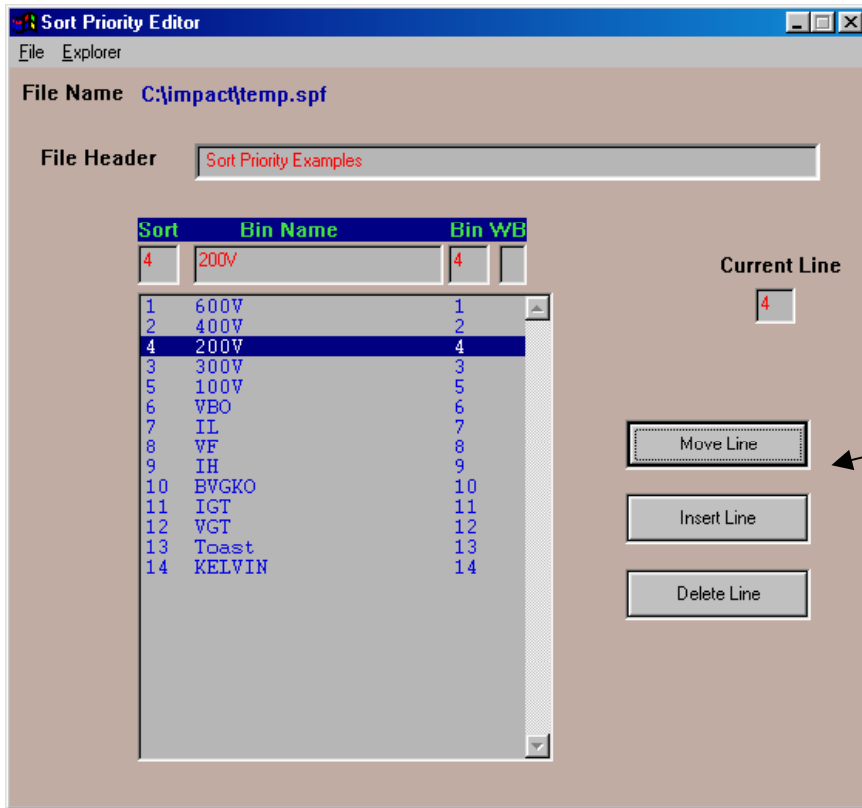
Great for presentation purposes when data has to be condensed from a larger file

Very useful to accommodate changes to files during a hi rel run.

Change Serial #, Lot, Sort, Bin, Results, and measurement units

Delete, Move and Copy Line Feature

Sort Priority Editor Window



Allows user to redefine or reorder the TBS sort priorities.

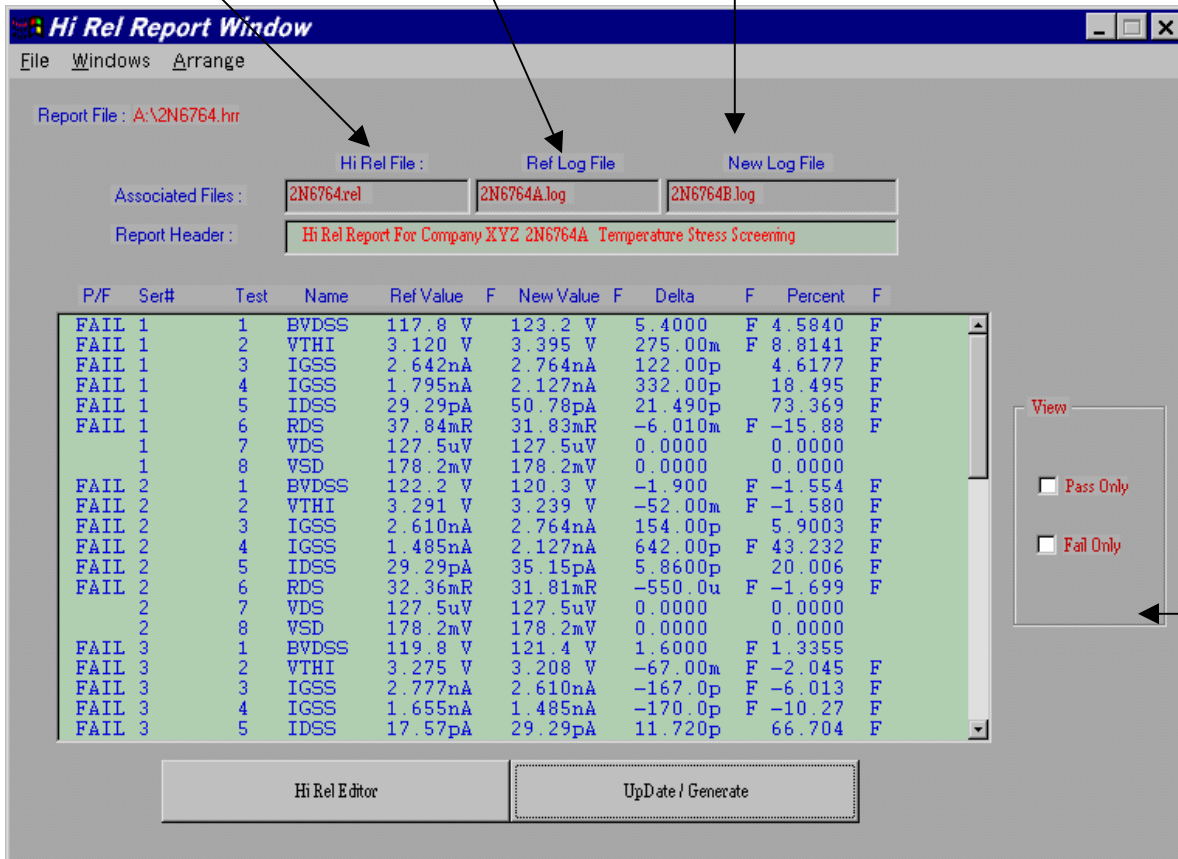
Easily Move, Insert or Delete Sort Line

Hi Rel File

Ref Log File

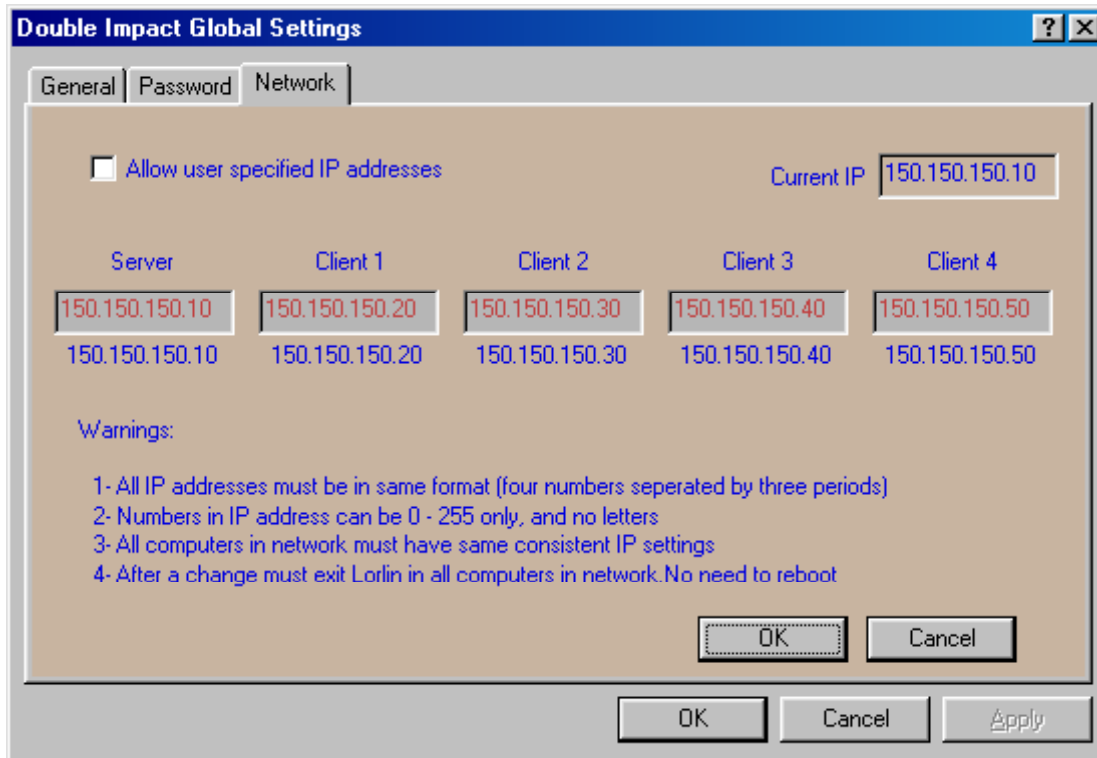
New Log File

Hi Rel Report



Report Generator for Pre and Post Test Results on Devices that have been treated, stressed, or subject to other environmental extremes.

Pass Only, Fail Only Feature

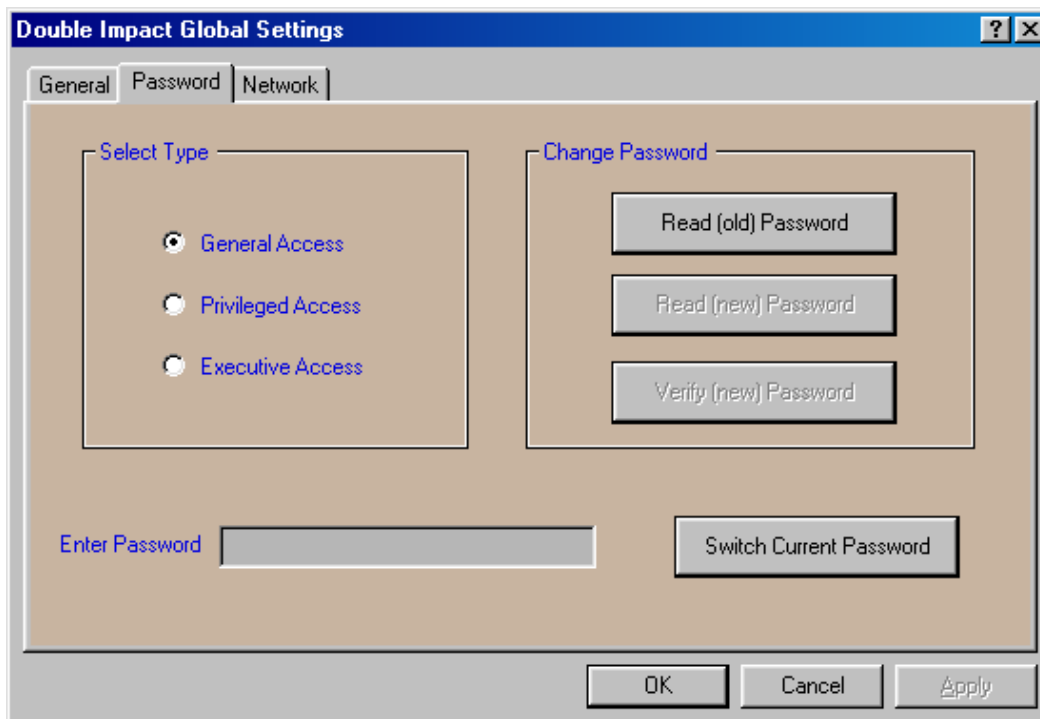


Networking Window

Network Computers to Share Files and Data.

Only One Computer is needed to run all five test stations.

The user can add a PC at each test station if desired by using the network features.



Password Window

Set up system passwords on three levels.

Restricts system users to various areas of the software.

Measurement Techniques:

System measurement techniques, refined and proven by years of field experience, accommodate a wide range of devices. Both high speed scanning and successive approximation methods are used to test devices. The method, type of test and the level of power are considered for each device parameter, and the best method is selected automatically by the system. In general, for low current tests such as leakage, the power is applied, the device is subjected to a "soak" period, and the high speed scan method which requires a few milliseconds is used. For high current measurements such as Common Emitter Current Gain, the power is applied for short periods of time, and the successive approximation method is used. The dwell time between the successive tests is adjusted automatically to keep the average power from adversely affecting the measurement of the device under test.

For all but low current measurements, which require a 'soak' period, power is removed immediately from the device under test when a decision is reached. Initial bias conditions are imposed which begin the tests as a pass, and the power is removed as soon as a failure is detected. This safeguard assures that the power is applied for no longer than necessary to perform the measurement accurately.

By considering each type of test and the operating current levels individually, the testing times and techniques are adjusted as described to provide extremely accurate measurements over the entire measuring range of the equipment. Kelvin connections are used throughout the system. In addition to the 3 current and 3 voltage sensing contacts at each test socket, this design has been incorporated into the circuitry on the high current printed circuit boards. Extensive shielding and guarding techniques assure accurate low level measurements. (These features have not been included in the simplified block diagrams.)

LEAKAGE CURRENT

A simplified diagram for performing **Leakage Current Measurement** is shown in Figure 1. A digital-to-analog converter provides a precision drive voltage for the High Voltage Test Supply. The Test Supply consists of an operational amplifier and high voltage booster circuit within the control loop. The programmed output voltage can be applied to any lead of the device under test. The two voltage ranges, which change the input resistor are selected by control circuits. The operating current range is evaluated, and current limiting resistors are selected automatically. The input of a high quality operational amplifier converts the Leakage Current to a proportional voltage and is connected to any lead of the device under test. The conversion factor is set by the value of feedback resistor, and eight ranges are available. A test-limit reference voltage is generated by another identical digital-to-analog converter, and the output is summed with the output of the current-to-voltage converter at the comparator input. The comparator is referenced to ground, and the output polarity will indicate the test decision.

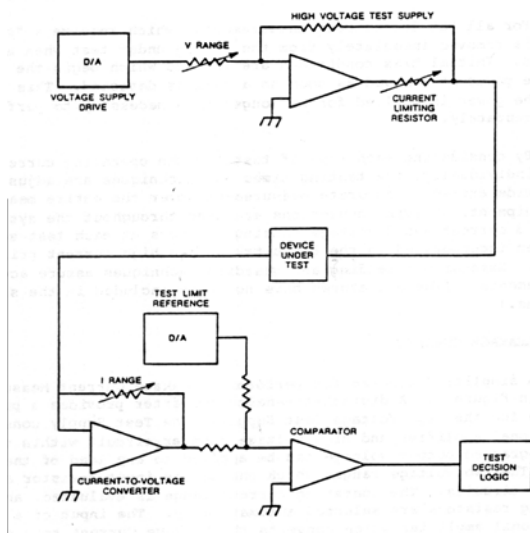


Figure 1

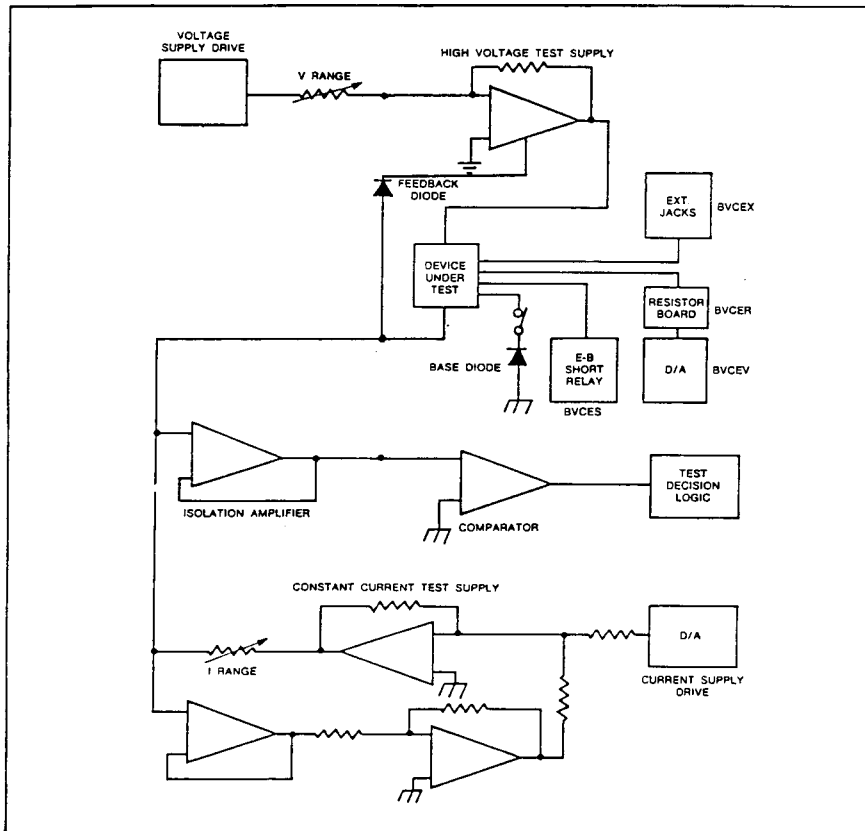
Reed relays are used to set the current range, the value of current limiting resistors and the interconnections of the Test Supplies with the device under test and the comparator. The supplies are programmed at computer speeds within a current range. Two digital-to-analog converters are on a single board. The entire high voltage supply is contained on one board, and the comparator, current converter and configuration interconnection relays are placed together on another board. For datalogging, the output of the test-limit reference is varied. High speed scan methods are used for currents up to 200 microamps, and successive approximation methods are used above that figure. The system will range automatically 2 decades above the programmed go/no-go limit and then will indicate OVER RANGE, or will range down one range and then datalog. Expanded up and down ranging is available as well.

BREAKDOWN VOLTAGE

To the left is a simplified diagram illustrating the methods used to perform **Breakdown Voltage measurements.**

A digital-to-analog converter supplies a precision drive voltage to the High Voltage Test Supply. The Test Supply consists of an operational amplifier and high voltage booster circuit within the control loop. The programmed output voltage can be applied to any lead of the device under test. The two voltage ranges are selected by logic circuits, which change the input resistor.

Another, identical, digital-to-analog converter supplies the drive for a Constant Current Test Supply. The output is also connected to any device lead. This point is at zero potential when the circuit is at a go/no-go decision, and the presence of a voltage will indicate either a pass or fail, depending upon polarity. An isolation amplifier with unity gain senses the voltage and feeds it to the comparator, which is referenced to ground. The output swing of the comparator is interpreted as a pass or fail by the Test

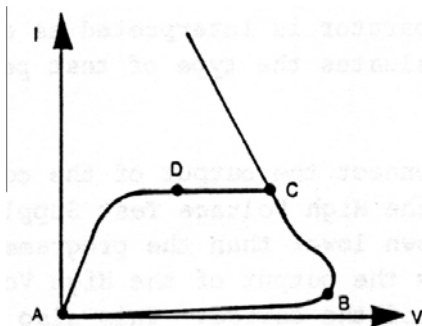


Decision Logic, which evaluates the type of test performed and the type of device.

Feedback diodes connect the output of the constant current supply to a control point in the High Voltage Test Supply. In the event the device under test has a breakdown lower than the programmed voltage, negative feedback is produced which limits the output of the High Voltage Supply to slightly more than the true breakdown of the device. This also limits the circuit current to essentially no greater than the programmed current.

The BVCEO measurement on transistors requires special consideration. Most devices exhibit a snap back characteristic during breakdown which produces a negative resistance region through which the operating point must normally pass. The figure below shows a typical collector characteristic plot. When power is applied, the path of the operating point is indicated by points A, B and C, where point C is the desired point of measurement. Since the negative resistance region is prone to oscillation difficulties, it is highly desirable to avoid this area and to follow path A, 0 and C. Then, as an additional benefit, the voltage capability of the High Voltage Supply has to accommodate only the operating point and not the peak breakdown voltage of the device.

Diodes connect the base of the device to ground for the BVCEO measurement. First, the current supply is turned on, and then the voltage supply is activated. If the breakdown voltage of the device is greater than the programmed value of the high voltage supply, the emitter of the device under test remains opposite in polarity of the collector. This maintains the forward bias of the base diode, and the device is biased in a common-base mode. Path A to D is followed, and the operating point occurs at D. The negative resistance path is avoided, and a good device as described will not enter a breakdown mode. If the breakdown voltage is less than the programmed limit, the device breaks down, the emitter is the same polarity as the collector, the base diode is reversed biased and the operating point progresses from D to C. Although the device may oscillate, the test will have been determined a failure because of the polarity sensed at the emitter by the isolation amplifier.

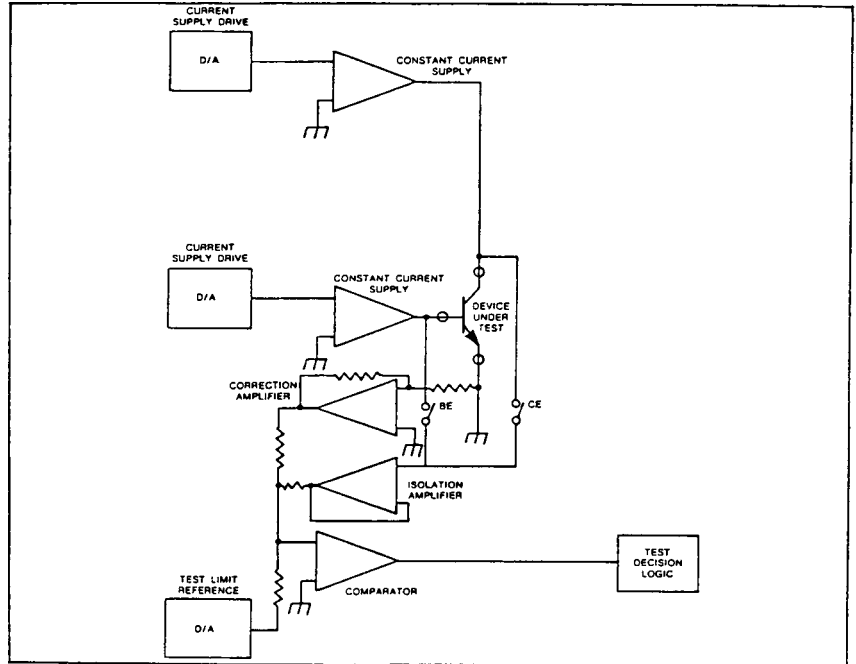


For BVCEV measurements, a resistor is selected from the resistor board and connected between the base and emitter of the device under test. For BVCEV measurements, a D/A converter is connected to the base of the DUT which is programmed for the desired value and polarity of the base voltage. A relay shorts the base to emitter for BVCES measurements and the external jacks at each test station are connected to all three leads of the device.

COMMON-EMITTER CURRENT GAIN (HFE) and SATURATION VOLTAGES

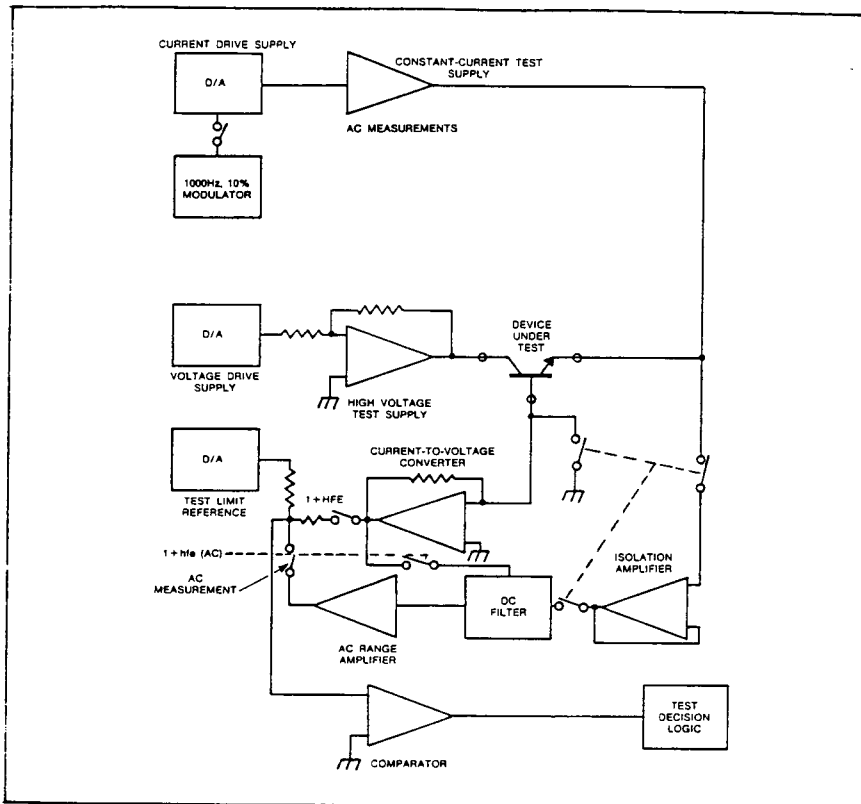
The tests available are: $V_{CE(SAT)}$, $V_{BE(SAT)}$, Base-to-Emitter, Linear Operating Voltage ($V_{BE ON}$), and Inverted Current Gain (INV. HFE).

The simplified circuit diagram for the Common-Emitter three-terminal measurements of transistors is shown. The two digital-to-analog converters supply the drive voltages for two identical constant-current supplies, which provide the programmed collector and base currents. To further simplify the diagram, the constant-current supplies are less detailed than in the previous pictures. When performing HFE or $V_{CE(SAT)}$ measurements, the unity-gain isolation amplifier has its input connected to the collector of the device under test, and its output of the summing junction of the comparator. Another digital-to-analog converter is programmed for the test limit reference voltage, and it is also connected to the comparator summing junction. The collector voltage is sensed and compared to the programmed test limit to determine if the test has been passed or failed. The voltage drop, because of high currents in the emitter wiring, is sensed and compensated for by the correction amplifier which provides a proportional input to the comparator summing junction.



For $V_{BE(SAT)}$ measurements, the input of the isolation amplifier is switched from the collector to the base of the device under test, and the measurement is performed in a similar manner. For $V_{BE(ON)}$ measurements, the base current is measured at the desired collector current and voltage bias conditions, and then a V_{BE} saturation measurement is performed using this value of base current. The collector and emitter terminals are interchanged to perform an inverted test.

COMMON BASE CURRENT GAIN ($1 + H_{FE}$), AC (1 kHz)



The test available are: Current Gain ($1+H_{FE}$), and Common Base Input Impedance (HIB).

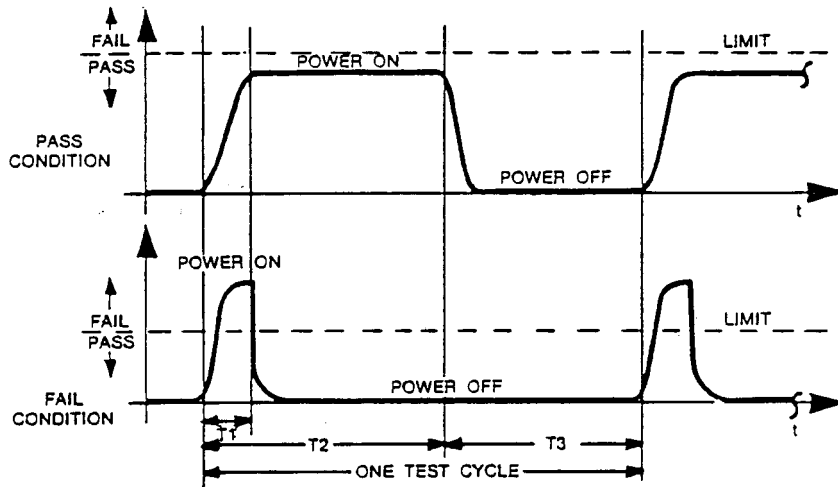
The simplified circuit diagram for the common-base current gain and 1-kHz measurements are shown below. Two digital-to-analog converters supply the individual precision drive voltages to a Constant-Current Test Supply and the High Voltage Test Supply. The Constant-Current Supply provides the emitter bias current for the device under test, and the High Voltage Supply provides the collector-to-base bias voltage. The current-to-voltage converter senses the base current and maintains the base at zero potential. For $1+H_{FE}$ dc measurements, the output is fed to the comparator input and compared with the test limit reference. The output polarity of the comparator is the test decision.

For 1+HFE ac measurements, the emitter current is modulated with a 1-kHz signal which is always exactly 10 percent of the programmed value. The Current-to-Voltage Converter senses both the ac and dc components of the base current. At the output, the dc component is filtered out and the ac signal is amplified and connected to the comparator input. The ac signal is compared to the test limit reference, and in this application, the comparator serves as a peak detector.

For HIB measurements, an Isolation Amplifier senses the emitter voltage and connects it to the input of the filter. The dc component is filtered out, the ac signal is amplified and connected to the comparator input. It is compared to a programmed output of the Test Limit Reference, and a test decision is made. The computer performs the mathematical division of the measured value of VEB and the programmed value of IE to generate the test decision. For HIE the same procedure is followed but now the system datalogs and retains the VEB and IB for the HIE calculation.

Test Times

The following chart shows the test times which are automatically programmed by the software.



An explanation of the test times follows:

TIME 1 (T1) Status-Gate Delay. The Status-Gate Delay is the amount of time during which power is applied to the device under test before a pass/fail decision is attempted. This time ensures that all forcing supplies have reached their programmed values to their listed specifications, all measuring circuits have either charged or discharged, the associated circuit transients have died out, and device capacitances have either charged or discharged to their final values before a pass/fail decision is attempted.

TIME 2 (T2) Power-On Time. The Power-On Time is the maximum total time that power may be applied to the device under test if the device passes the programmed test. At the end of T1, the comparator circuits are enabled, and if the device fails at any time before the termination of T2, the power will be automatically removed. Effectively, the comparator is enabled for a time which is equal to T2 minus T1. This allows the system to indicate a failure for a device which is unstable during measurement times if the device drifts into the Fail region.

TIME 3 (T3) Post-Test Delay. This post-test delay is a POWER OFF condition after T2 and is incorporated when high or medium-power levels exist due to the programmed currents and voltage. The post-test delay allows the device sufficient time to cool off before another test measurement is made. This ensures that device heating does not appreciably alter the measured parameter.

INTERPRETATIONS OF TEST-TIME CHARTS

To find the test times used for any test at any level, examine each of the charts (group 1, group 2, group 3 and ac tests) that follow. Look for the appropriate test and look down the left-hand column for the programmed current; read across to find times T1, T2 and T3. For example, a 15-ampere HFE test is in group 1, and has T1=300 microseconds, T2=400 microseconds and T3=16 milliseconds. For a BVCBO at 100 microamps of IB, refer to the group 2 tests and find the row which indicates the programmed current from 18 microamps to 180 microamps, resulting in T1=3 mS, T2=6 mS, T3=0. For all groups at the extreme lower current levels, the pass/fail decision is made 50 microseconds before power is removed.

GROUP 1 TESTS

Group 1 tests: HFE, HFEIB, DELTA HFE, VCESAT, VBESAT, VBEON, BVZ, VF

Collector Current	Time 1* Status-Gate Delay	Time 2* Total Power On	Time 3* Post-Test Delay
1.8005 A to 20.0 A	300 uS	400 uS	16 mS
180.05 mA to 1.80 A	300 uS	600 uS	8 mS
18.005 mA to 180 mA	500 uS	1 mS	4 mS
1.8005 mA to 18 mA	2 mS	4 mS	0
180.05 uA to 1.80 mA	3 mS	6 mS	0
18.005 uA to 180 uA	4 mS	8 mS	0
1.8005 uA to 18.0 uA	19.95 mS	20.0 mS	4 mS
180.05 nA to 1.80 uA	49.95 mS	50.0 mS	4 mS
0 to 180.05 nA	99.95 mS	100.0 mS	4 mS

* +20%

For ac testing (1 kHz), all ranges use the same test times of T1=10 mS, T2=12 mS and T3=10 mS, overriding the test-word printout of the times in words 9 and 10 (10 words/test). Test times do not include ramp times or other supply sequence times.

The test-time charts show sequences suitable for incoming inspection and engineering evaluation applications. Test-times are adjustable for individual applications

DATALOGGING TIMES

The system automatically adjusts its test times according to the measurement range used. For example, if an ICBO of 1 mA is programmed, then T1=500 microseconds, T2=1 mS and T3=4 mS. If the unit had an actual ICBO of 1.5 microamps, then the system would automatically downrange and adjust the test times for T1=4 mS, T2=8 mS and T3 = 0. Conversely, if the measured current is greater than the programmed value, the system decreases the times due to the increased power levels.

Group 2 tests: All BV except BVZ

Collector Current	Time 1* Status-Gate Delay	Time 2* Total Power On	Time 3* Post-Test Delay
180.05 mA to 500 mA (BV only)	300 uS	400 uS	16 mS
18.005 mA to 180 mA (BV only)	300 uS	600 uS	8 mS
1.8005 mA to 18 mA	500 uS	1 mS	4 mS
180.05 uA to 1.80 mA	2 mS	4 mS	0
18.005 uA to 180 uA	3 mS	6 mS	0
1.8005 uA to 18 uA	4 mS	8 mS	0
180.05 nA to 1.80 uA	19.95 mS	20 mS	4 mS
0 to 180.0 nA	49.95 mS	50.0 mS	4 mS

* +20%

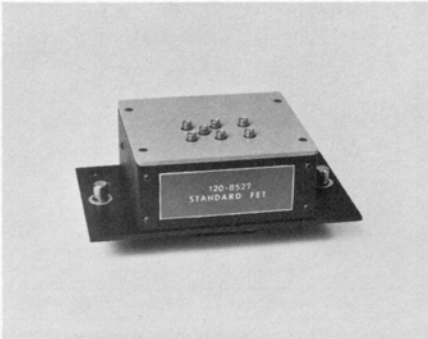
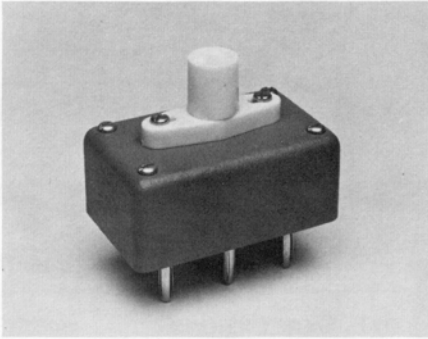
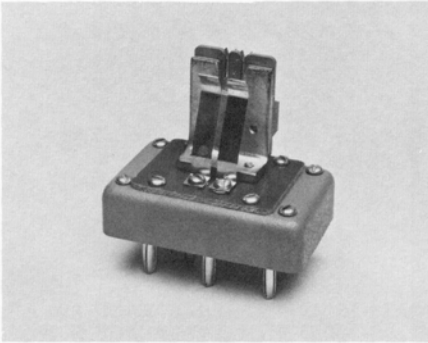
Group 3 tests: All I, 1+HFE, 1+HFEIB

Collector Current	Time 1* Status-Gate Delay	Time 2* Total Power On	Time 3* Post-Test Delay
18.005 mA to 180.0 mA	300 uS	400 uS	16 mS
1.8005 mA to 18.0 mS	300 uS	600 uS	8 mS
180.05 uA to 1.80 mA	500 uS	1 mS	4 mS
18.005 uA to 180.0 uA	2 mS	4 mS	0
1.8005 uA to 18.0 uA	3 mS	6 mS	0
180.05 nA to 1.80 uA	4 mS	8 mS	0
18.005 nA to 180.0 nA	19.95 mS	20 mS	4 mS
0 to 18.0 nA	49.95 mS	50.0 mS	4 mS

* +20%

Test Fixtures

Lorlin offers a wide variety of test fixtures for most discrete component packages. Blank fixture kits are offered for customers that have special devices or sockets and wish to build their own custom fixtures.



TO-92 EBC Transistor Test Fixture
TO-92 ECB Transistor Test Fixture
TO-92 CEB Transistor Test Fixture
TO-126/TO-202/TO-220 EBC Transistor Test Fixture
TO-126/TO-202/TO-220 ECB Transistor Test Fixture
DO-4/DO-5 Diode Test Fixture
DO-7/DO-13 (Tape and Reel) Diode Test Fixture
TO-5/TO-18/TO-39/TO-72 EBC Transistor Test Fixture
TO-3 Transistor Test Fixture
TO-66 Transistor Test Fixture
TO-5/TO-18/TO-39/TO-72 BEC Transistor Test Fixture
DO-7/DO-13 Clip Adapter and Clips (two clips required)
TO-5/TO-18/TO-39/TO-72 CBE Transistor Test Fixture
TO-5/TO-18/TO-39/TO-72 BCE Transistor Test Fixture
TO-5/TO-18/TO-39/TO-72 CEB Transistor Test Fixture
DO-7/DO-13 (Side to Side) Diode Test Fixture
TO-126/TO-202/TO-220 CEB Transistor Test Fixture
TO-126/TO-202/TO-220 BEC Transistor Test Fixture
SOT-23 EBC Transistor Test Fixture
SOT-23 BEC Transistor Test Fixture
TO-5/TO-18 ECB "in-Line" Transistor Test Fixture
TO-5/TO-18 EBC "in-Line" Transistor Test Fixture
Blank High Box (1.0")
Blank Low Box (0.5")
Blank High Box (1.5")
[Super Station Fixtures for SS100 and SS150](#)
DO-4/DO-5 Diode Test Fixture
DO-7/DO-13 (Side to Side) Diode Test Fixture
DO-7/DO-13 Clips (two required)
DO-7/DO-13 Clip Adapter
TO-3 Transistor Test Fixture
TO-5/TO-18/TO-39/TO-72 D4SG Transistor Test Fixture
TO-5/TO-18/TO-39/TO-72 4GSD Transistor Test Fixture

TO-5/TO-18/TO-39/TO-72 SDG4 or ECB Transistor Test Fixture
TO-5/TO-18/TO-39/TO-72 SGD4 or EBC Transistor Test Fixture

TO-66 Transistor Test Fixture

TO-92 GDS or SCE Transistor Test Fixture

TO-126/TO-202/TO-220 SDG or ECB Transistor Test Fixture

SS-100 Single Device Adapter

SS-100 Single Device Adapter (CAP)

SS-150 Single Device Adapter

SS-150 Single Device Adapter (CAP)

SS-200 7 Pin Test Fixture Adapter

TO-78 Dual FET/Bipolar SDG/SDG or CBE/EBC for SS-150 (station requires 2 matrix relay boards)

TO-78 Dual FET/Bipolar SDG/SDG or CBE/EBC for SS-150 with CAP (station requires 4 matrix relay boards)

6 Lead DIP Optocoupler AK/ECB for SS-100 (station requires 3 matrix relay boards)

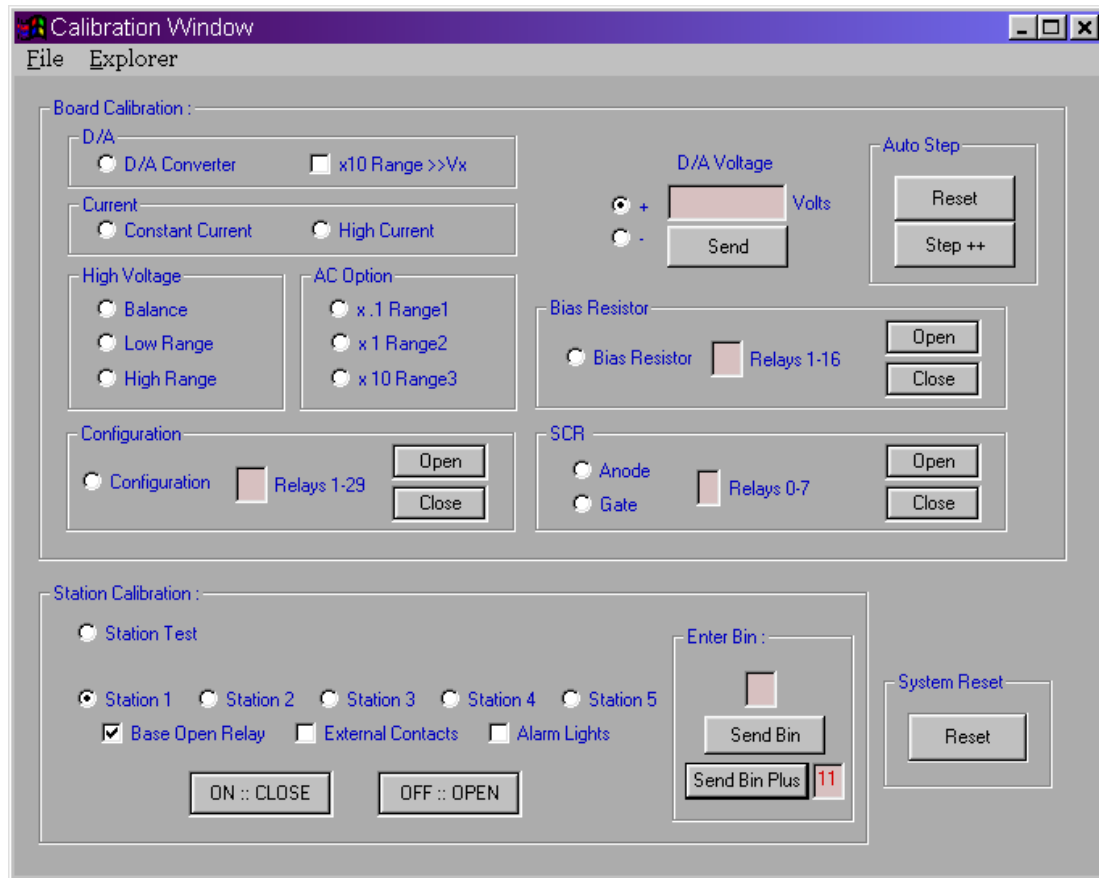
6 Lead DIP Optocoupler AK/ECB for SS-150 (station requires 3 matrix relay boards)

TO-78 Optocoupler for SS-150 (station requires 3 matrix relay boards)

Blank Adapter - 25 Pins for SS-100/SS-150

Calibration

A complete system calibration can be completed in less than one hour using the calibration window, a variable dc supply, and a digital voltmeter. The calibration adjustments include offset nulling of operational amplifiers and gain setting of the digital to analog converters.



TEST SPECIFICATIONS

TESTS/PARAMETERS		RANGE	MAX RESOLUTION	ACCURACY (*)
TRANSISTORS/DIODES/ZENERS				
ICBO,IEBO, ICE(O,S,V, R,X),IR	VOLTAGE	0V-600V (Note 1)	50mV	.5%+50mV+2mV/mA
	CURRENT	5pA-200mA	5pA (100 fA)**	.5%+100pA+2pA/V
	R	0K-20K	10Ω	1%+1Ω
	V	0V-80V**	5mV	.5%+5mV+2mV/mA
BVCBO, BVEBO, BVCE (O,S,V,R,X) BVR	VOLTAGE	0V-600V(Note 1)	50mV	.5%+50mV+2mV/mA
	CURRENT	2μA-1A	500pA	.5%+500pA
	R	0K-20K	10Ω	1%+1Ω
	V	0V-80V**	5mV	.5%+5mV+2mV/mA
BVZ	VOLTAGE	0V-15V(Note 2)	.5mV	.5%+1mV+1mV/A
	CURRENT	10μA-20A	5nA	.5%+50nA
	SOAK TIME	0S-30,000mS	10mS	10%
	SOAK I	10μA-180mA		
HFEIB, HFE, DHFE, HFEIC	COLLECTOR I	10μA-20A	5nA	.5%+50nA
	COLLECTOR V	0V-15V(Note 2)	.5mV	.5%+1mV+1mV/A
	BASE I	200nA-10nA	5nA	.5%+5nA
	GAIN	.1-10,000	.01	1%
1 + HFE, 1+ HFEIB	EMITTER I	10μA-1A	500pA	.5%+5nA
	COLLECTOR V	0V-600V(Note 1)	50mV	.5%+50mV+2mV/mA
	BASE I	20pA-200mA	5pA (100 fA)**	.5%+100pA+2pA/V
	GAIN	.1-100,000	.01	1%
VCESAT, VBESAT, VBEON,VF,	COLLECTOR I	10μA-20A	5nA	.5%+50nA
	BASE I	200nA-10A	5nA	.5%+5nA
	VOLTAGE	0V-15V(Note 2)	.5mV	.5%+1mV+1mV/A
FIELD EFFECT TRANSISTORS				
IDGO, IGSO IDSX, ISDX, IGSS, VTHI, VGSI, IGI, IGV	VOLTAGE	0V-600V(Note 1)	50mV	.5%+50mV+2mV/mA
	CURRENT	5pA-200mA	5pA (100 fA)**	.5%+100pA+2pA/V
	VOLTAGE (3rd Lead)	0V-80V**	5mV	.5%+5mV+2mV/mA
BVDGO, BVGSO, BVGSS, BVDSX	CURRENT	2μA-1A	500pA	.5%+500pA
	VOLTAGE	0V-600V(Note 1)	50mV	.5%+50mV+2mV/mA
	VOLTAGE (3rd Lead)	0V-80V**	5mV	.5%+5mV+2mV/mA
IDVV, VGSV, VDSV,RDS, GFS	CURRENT	200nA-20A	5nA	.5%+50nA
	VOLTAGE	0V-10V	.5mV	.5%+1mV+1mV/A
	VOLTAGE (3rd Lead)	0V-80V**	5mV	.5%+5mV+2mV/mA
AC (1 Khz) OPTION				
AC 1+HFE, AC HIB, GM (Note 3) AC HIE	DC			
	EMITTER I (Note 4)	100μA-20mA	50nA	.5%+100nA
	COLLECTOR V	1V-400V	.5V	.5%+50mV+2mV/mA
	AC 1+HFE	1-1000	.1	3%
	AC HIB	1Ω-1000Ω	.1	3%+3Ω
AC HIE	100Ω-100KΩ	1Ω	4%+(3Ω X ACHFE)	
<p>NOTES:</p> <p>1) 1A at 100V; derate linearly to 1mA at 600V.</p> <p>2) Limited to 10V above 1A.</p> <p>3) Programmed in transistor test terminology. GM= $\frac{1}{ACHIB}$</p> <p>4) AC Current: IAC=IDX x .1 AC VMeasure: 2mV-2V</p>				

* Accuracy specifications are in addition to +/- 1 digit in printout.

** Option Required

TEST SPECIFICATIONS (cont.)

TESTS/PARAMETERS		RANGE	MAX RESOLUTION	ACCURACY (*)
AC OPTION (1kHz) (cont.)				
ZZ (ZZT,ZZK)	DC CURRENT(Note 4)	20μA-180mA	.5nA	.5%+50nA
	VOLTAGE	1V-200V(Note 1)		
	IMPEDANCE	0Ω-10,000Ω	.1Ω	3%+5Ω
ZZL (ZZT,ZZK)	DC CURRENT(Note 4)	20μA-180mA	.5nA	.5%+50nA
	VOLTAGE	0V-16V		
	IMPEDANCE(Note 4)	0Ω-10,000Ω	.1Ω	3%+2Ω
SCR/TRIAC OPTION (Note 9)				
IAKR (Note 5)	VOLTAGE	0V-600V (Note 8)	50mV	.5%+50mV+2mV/mA
IAKF (Note 5)	CURRENT	5pA-200mA	5Pa (100 Fa)**	.5%+100pA+3pA/V
IGKO				
BVAKR (Note 5)	CURRENT	2μA-1A (Note 1)	500Pa	.5%+500pA
BVAKF (Note 5.7)	VOLTAGE	0V-600V	50mV	.5%+50mV+2mV/mA
BVGKO				
IGT (Note 6)	ANODE I	10μA-2A	10nA	.5%
	GATE I	±(200nA-200mA)	.5nA	.5%+5nA
VGT (Note 6)	ANODE I	10μA-2A	10nA	.5%
	GATE V	±(0V-5V)	5mV	.5%+5mV
	GATE I	100mA max.		
IH (Note 5,.6)	INITIAL GATE I	2μA-200mA	.5nA	.5%+2nA
	FINAL GATE I	±(2μA-200mA)	.5nA	.5%+2nA
	INITIAL ANODE I	2X HOLDING I		
	HOLDING I	10μA-100mA	5nA	.5%+1μA
IL (Note 5,.6)	INITIAL GATE I	±(2μA-200mA)	.5nA	.5%+2nA
	FINAL GATE I	±(2μA-200mA)	.5nA	.5%+2nA
	LATCHING I	20μA-200mA	5nA	.5%+2μA
VON	ANODE I	10μA-20A	5nA	.5%
	INITIAL GATE I	±(20μA-2A)	5nA	.5%+5nA
	ON-STATE V	0V-10V	.5mV	.5%+1mV+1mV/A
<p>NOTES:</p> <p>1) 1A at 100V; derate linearly to 1mA at 600V.</p> <p>5) RGK is programmable in 10Ω steps from 0Ω -20,000Ω .</p> <p>6) Programmable positions are available for customer RC Networks and/or zener clamps for control of rise times, noise filterings, and dynamic impedance.</p> <p>7) BVAKF range is 1mA to 500mA.</p> <p>8) 200Ma at 0V-300V; derate linearly to 1mA at 600V.</p> <p>9) Specifications apply to testing using an OTS-100 station.</p>				

TEST STATION OPTIONS

TESTS/PARAMETERS		RANGE	MAX RESOLUTION	ACCURACY (*)
HVS-102 - HIGH VOLTAGE STATION				
LEAKAGE	VOLTAGE	200V-2000V(Note 1)	500mV	.5%+500mV+3mV/mA
	CURRENT	5pA-75mA (Note 2)	5pA	.5%+500pA+6pA/V
BREAKDOWN	CURRENT	2μA-75mA (Note 2)	500pA	.5%+2nA
	VOLTAGE	200V-2000V (Note 1)	500mV	.5%+500mV+3mV/mA
<p>NOTES:</p> <p>1) Not available for PNP transistors.</p> <p>2) 75mA from 200v-1000v; derate linearly to 1mA at 2000V.</p> <p>GENERAL NOTES: All other tests: Accuracy - Twice the normal tag error and sensitivity.</p>				

* Accuracy specifications are in addition to +/- 1 digit in printout.

** Option Required

TEST SPECIFICATIONS (cont.)

TESTS/PARAMETERS		RANGE	MAX RESOLUTION	ACCURACY (*)
HCM-100 - HIGH CURRENT OPTION (Note 1) For Main Deck OTS-100 or HPTS-50				
GROUNDING EMITTER TESTS	COLLECTOR I COLLECTOR V	20A-100A 0V-10V	50mA .5mV	1%+50mA .5%+1mV+1mV/A
LEAKAGE CURRENT				.5%+5nA+1nA/V
NOTES: 1) High Current Option available at 1-4 stations.				
CAPACITANCE MEASUREMENT OPTION				
COB (Note 2) CIB	TEST FREQUENCY TEST SIGNAL LEVEL	1mHz 100mV RMS	FIXED FIXED	.5%+50mV+3mV/mA 2%+1pF
CRSS (Note 2) CISS	BIAS CAPACITANCE	0V-±50V (Note 3) 0-100pF	50mV .1pF	
<p>NOTES:</p> <p>OTS</p> <p>1) Requires one or more of the following station options: A: OTS-130 for 3 terminal devices, 6A DC maximum. B: OTS-131 for 2 terminal devices, 1.8A DC maximum. C: Super Station Capacitance Option. D: OTS-230 High Voltage Cap Station.</p> <p>2) Mutually exclusive tests. CRSS in Super Stations only, COB in only.</p> <p>3) Bias: 0v-±20V Resolution: 5mV Accuracy: .5%+5mV+3mV/mA</p>				
TESTS/PARAMETERS		RANGE	MAX RESOLUTION	ACCURACY (*)
SS-100 - SUPER STATION OPTION **				
LEAKAGE CURRENT		5pA-200mA	5pA	.5%+100pA+2pA/V plus 100pA+2NpA/V where N equals number of relay boards or equivalent. (Note 2)

* Accuracy specifications are in addition to +/- 1 digit in printout.

TEST SPECIFICATIONS (cont.)

TESTS/PARAMETERS		RANGE	MAX RESOLUTION	ACCURACY (*)
SS-150 OPTION - FET STATION				
LEAKAGE TESTS				
IGCC,IGV, IGDO,IGSO, IDSX,ISDX, ISVI,IGI, VGS1,VTHI	VOLTAGE CURRENT (Standard) CURRENT (Low Leakage) VG	0V-600V(Note 2) 5pA-200mA 0A-200pA, 2nA,20nA 0V-80V	50mV 5pA 100fA 5mV	.5%+50mV+3mV/mA .5%+100pA+.5pA/V 2%+5pA+.1pA/V(Note 3) .5%+5mV+2mV/mA
BREAKDOWN TESTS				
BVDSX,BVGSS, BVGDO,BVGSO VSVG,VGSB, ISVB	CURRENT VOLTAGE VG	2μA-1A(Note 2) 0V-600V 0V-80V	50nA 50mV 5mV	.5%+50nA .5%+50mV+3mV/mA .5%+5mV+2mV/mA
ON CHARACTERISTICS				
VDSV,VGSF, VGSSF,VGSV, IDVV,RDS, GFS	CURRENT VOLTAGE VG RDS GFS	2μA-1.8A 0V-15V 0V-80V 0Ω-4095Ω 1mmho-10mho	50nA .5mV 5mV	.5%+50nA .5%+1mV+1mV/A .5%+5mV+2mV/mA
OTHER TESTS				
ACRDS, ACGOS(Note 4)	DC CURRENT (Note 5) VOLTAGE VG ACRDS	20μA-20mA 0V-15V 0V-80V 0Ω-10,000Ω	5nA .5mV 5mV .1Ω	.5%+50nA .5%+1mV+1mV/A .5%+5mV+2mV/mA 3%+3Ω
ACGFSV, ACGFSI, ACGFS (Note 4)	VOLTAGE DC CURRENT (Note 5) VG GFS	0V-400V 20μA-20mA 0V-80V 100μmho-1mho	50mV 50nA 5mV	.5%+50mV+3mV/mA .5%+100nA .5%+5mV+2mV/mA
CISS,CRSS (Note 6)	VOLTAGE CAPACITANCE	0V-150V(Note 7) 0F-100pF	50mV .1pF	.5%+50mV+3mV/mA 2%+1pF
<p>NOTES:</p> <p>1) FET test names also available without SS-150 Option.</p> <p>2) Maximum Voltage =600V. 1A at 100V; derate linearly to 1mA at 200V.</p> <p>3) If the capacitance option is included, the leakage accuracy is: 2%+10pA+.2pA/V.</p> <p>4) Available with AC (1kHz) Option.</p> <p>5) AC Current: IAC=IDC x .1 / AC VMEASURE: 2mV-2V</p> <p>6) Available with capacitance option on SS-150 station.</p> <p>7) Bias: 0v-±20V Resolution: 5mV Accuracy: .5%+5mV+3mV/mA</p>				

* Accuracy specifications are in addition to +/- 1 digit in printout.

TEST SPECIFICATIONS OPTIONS (cont.)

TESTS/PARAMETERS		RANGE	MAX RESOLUTION	ACCURACY (*)
OTS-201 MANUAL HIGH VOLTAGE/HIGH CURRENT TEST STATION (with HVS-201 voltage source and HCM-101 current source) (and OTS221, OTS225)				
ALL LEAKAGE TESTS	VOLTAGE CURRENT	0V-600V(Note 1) 5pA-200mA	50mV 5pA	.5%+50mV+3mV/mA .5%+400pA+4pA/V
HIGH VOLTAGE MODE	COLLECTOR V	200V-2000V (Note 2,3)	500mV	.5%+500mV+10mV/mA
BREAKDOWN VOLTAGE TEST (High Voltage Mode)	VOLTAGE CURRENT	200V-2000V (Note 2) 2μA-75mA) (Note 3)	500mV 500pA	.5%+500mV+3mV/mA .5%+2nA
GROUNDING EMITTER TESTS	COLLECTOR I	20.05A-100A (160A-200A) Note 4	50mA	1%+50mA
<p>NOTES: 1) 1A at 100V; derate linearly to 1mA at 600V. 2) Not available for PNP transistors 3) 75mA from 200V-1000V; derate linearly to 1mA at 2000V 4) OTS221 provides 160 Amps, OTS225 Provides 200 Amps</p> <p>GENERAL NOTES: All other tests: Accuracy - Twice the normal tag error and sensitivity.</p>				
TESTS/PARAMETERS		RANGE	MAX RESOLUTION	ACCURACY (*)
OTS-300/340 and HCS-500 Test Station				
	CURRENT (in one range)	20.05A-200A(400-500A) Note 2	50mA	1%+50mA
	VOLTAGE	0V-10V(Note 1)	.5mV	.5%+1mV+1mV/A
ALL LEAKAGE TESTS	VOLTAGE CURRENT	0V-600V 5pA-200mA	50mV 5pA	.5%+50mV+3mV/mA .5%+5nA+1nA/V
<p>NOTES: 1. The ability to supply 10V at 200A is dependent on the input AC-line voltage and is not guaranteed over the entire system operating range. 5) OTS340 provides 400 Amps. HCS-500 provides 500 Amps.</p> <p>GENERAL NOTES: All other tests: Range - Standard ranges Accuracy - Twice the normal tag error and sensitivity.</p>				
<p>NOTES: 1) 1A at 100V; derate linearly to 1mA at 600V. 2) OTS401 provides 2000V, 10A capability with HVS 201 Supply</p> <p>GENERAL NOTES: VCC Source: Range - Adjustable 1.25V-20V (max recommended load 50mA) All other tests: Range - Standard ranges (max recommended current IE/IC=5A, IB=1A)</p>				

* Accuracy specifications are in addition to +/- 1 digit in printout.
ALL SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE
**** Option Required**

POWER SUPPLY COMPLIANCE CHARTS

